

CLAIMS

What is claimed is:

- 1 1. A memory system comprising:
 - 2 a plurality of memory devices coupled one to another in a chain;
 - 3 a memory controller coupled to the chain and configured to output a memory access
 - 4 command that is received by each of the memory devices in the chain and that selects
 - 5 a set of two or more of the memory devices to be accessed.
- 1 2. The memory system of claim 1 wherein the memory access command is a memory read
- 2 command that selects a set of the memory devices to be read by the memory controller;
- 1 3. The memory system of claim 1 wherein the memory access command is a memory write
- 2 command that selects a set of the memory devices to store a sequence of write data values.
- 1 4. The memory system of claim 1 wherein the set of memory devices comprises fewer than
- 2 all the memory devices in the chain.
- 1 5. The memory system of claim 1 wherein each of the memory devices in the chain, except a
- 2 last memory device, comprises an output port coupled to an input port of another of the
- 3 memory devices.
- 1 6. The memory system of claim 5 wherein a first memory device in the chain comprises an
- 2 input port coupled to the memory controller to receive the access command.
- 1 7. The memory system of claim 6 wherein the memory controller is coupled to the input port

2 of the first memory device in the chain via a point-to-point signaling path.

1 8. The memory system of claim 7 wherein the output port of each memory device in the
2 chain, except the last memory device, is coupled to the input port of one other of the
3 memory devices via a point-to-point signaling path.

1 9. The memory system of claim 5 wherein the last memory device comprises an output port
2 coupled to an input port of the memory controller.

1 10. The memory system of claim 1 wherein each of the memory devices in the chain comprises
2 an interface register having a buffer input and a buffer output, the buffer output of each of
3 the memory devices, except a last memory device in the chain, being coupled to the buffer
4 input of one other memory device in the chain via a respective point-to-point signaling
5 path.

1 11. The memory system of claim 10 wherein each of the memory devices in the chain
2 comprises a clock signal receiver coupled to receive a clock signal and having an output
3 coupled to a strobe input of the interface register.

1 12. The memory system of claim 11 wherein the interface register within each of the memory
2 devices is configured to store a value present at the buffer input in synchronism with each
3 rising edge transition of the clock signal.

1 13. The memory system of claim 12 wherein the interface register within each of the memory
2 devices is further configured to store a value present at the buffer input in synchronism
3 with each falling edge transition of the clock signal.

1 14. The memory system of claim 11 wherein the interface register within each of the memory
2 devices is configured to store a value present at the buffer input in synchronism with each
3 falling edge transition of the clock signal.

1 15. The memory system of claim 11 wherein each of the memory devices further comprises a
2 clock output driver having an input coupled to an output of the clock receiver and output
3 coupled to an input of the clock signal receiver within another one of the memory devices.

1 16. The memory system of claim 10 wherein the interface register comprises a first plurality of
2 edge-triggered storage elements each having a strobe input coupled to receive a clock
3 signal.

1 17. The memory system of claim 16 wherein the interface register further comprises a second
2 plurality of edge-triggered storage elements each having a strobe input coupled to receive a
3 complement of the clock signal.

1 18. The memory system of claim 14 wherein each of the memory devices in the chain further
2 comprises an output data buffer and a select circuit, the select circuit having a first input
3 port coupled to the output data buffer, a second input port coupled to the interface register
4 and, in each of the memory devices in the chain except the last memory device, an output
5 port coupled to the buffer input of the interface register of the one other memory device.

1 19. The memory system of claim 1 wherein each of the plurality of memory devices is a
2 discrete integrated circuit device.

- 1 20. The memory system of claim 1 further comprising a substrate and wherein at least a
- 2 portion of the memory devices are mounted to the substrate.
- 1 21. The memory system of claim 20 further comprising sets of conductive traces formed on the
- 2 substrate and coupled between respective pairs of the memory devices mounted on the
- 3 substrate.
- 1 22. The memory system of claim 1 further comprising a substrate having first and second
- 2 surfaces, and wherein a first portion of the memory devices are mounted on the first surface
- 3 of the substrate, and a second portion of the memory devices are mounted on the second
- 4 surface of the substrate.
- 1 23. The memory system of claim 22 further comprising:
 - 2 a first sets of conductive traces coupled between respective pairs of the memory devices
 - 3 mounted on the first surface of the substrate; and
 - 4 a second sets of conductive traces coupled between respective pairs of the memory devices
 - 5 mounted on the second surface of the substrate.
- 1 24. The memory system of claim 23 further comprising a set of conductive traces extending
- 2 from one of the memory devices mounted on the first surface to one of the memory devices
- 3 mounted on the second surface.
- 1 25. The memory system of claim 22 further comprising an interconnection structure coupled to
- 2 the memory controller, the substrate being removably coupled to the interconnection
- 3 structure.

- 1 26. A method of operation in a memory controller, the method comprising:
 - 2 receiving a memory access request that specifies a range of memory addresses;
 - 3 outputting a memory access command to a plurality of memory devices coupled one to
 - 4 another in a chain, the memory access request including selection information, based
 - 5 on the specified range of memory addresses, that selects a set of two or more of the
 - 6 memory devices to be accessed.
- 1 27. The method of claim 26 wherein the memory devices in the chain are associated with
- 2 respective memory identifiers, and wherein the selection information indicates at least two
- 3 of the memory identifiers.
- 1 28. The method of claim 27 wherein each of the memory identifiers indicates a position, within
- 2 the chain, of the associated memory device, and wherein the selection information
- 3 comprises a start memory identifier and an end memory identifier that collectively select
- 4 all the memory devices disposed within the chain between the memory devices associated
- 5 with the start and end memory identifiers.
- 1 29. The method of claim 28 wherein the start memory identifier and end memory identifier
- 2 additionally select the two memory devices associated with the start and end memory
- 3 identifiers.
- 1 30. The method of claim 26 wherein the memory access request is a read request and wherein
- 2 the memory access command is a read command.
- 1 31. The method of claim 30 further comprising outputting a read-data pickup command to the

2 plurality of memory devices after outputting the memory access command.

1 32. The method of claim 31 wherein outputting a read-data pickup command comprises
2 outputting a read-data pickup command that includes the selection information that was
3 included in the memory access command.

1 33. The method of claim 31 further comprising receiving read data from the set of the memory
2 devices selected by the selection information.

1 34. The method of claim 31 wherein outputting a read-data pickup command after outputting
2 the memory access command comprises delaying, after outputting the memory access
3 command, for a predetermined number of cycles of a clock signal before outputting the
4 read-data pickup command.

1 35. The method of claim 34 wherein delaying for the predetermined number of cycles of the
2 clock signal comprises retrieving a delay value indicative of the predetermined number of
3 cycles of the clock signal from a storage location within the memory controller.

1 36. The method of claim 35 wherein retrieving the delay value from the storage location
2 comprises retrieving the delay value from one of a plurality of storage locations within the
3 memory controller according to the set of the memory devices to be accessed.

1 37. The method of claim 36 further comprising reading parameter data from each of the
2 memory devices in the chain during a configuration operation, generating the delay value
3 based on the parameter data and storing the delay value in the one of the plurality of
4 storage locations.

- 1 38. The method of claim 26 wherein the memory access request is a write request and wherein
2 the memory access command is a write command.
- 1 39. The method of claim 38 further comprising:
2 receiving a plurality of write data values within the memory controller; and
3 outputting the plurality of write data values, one after another, to the plurality of memory
4 devices.
- 1 40. The method of claim 39 wherein outputting the plurality of write data values to the
2 plurality of memory devices comprises outputting the plurality of write data values after
3 outputting the write command.
- 1 41. The method of claim 40 wherein outputting the write command to the plurality of memory
2 devices comprises outputting the write command to a first memory device in the chain via
3 a point-to-point signaling path, and wherein outputting the plurality of write data values
4 after outputting the write command comprises outputting the plurality of write data values,
5 one after another, to the first memory device via the point-to-point signaling path.
- 1 42. The method of claim 26 wherein outputting the memory access command to the plurality of
2 memory devices coupled in a chain comprises outputting the memory access command to a
3 first memory device in the chain, the first memory device being configured to receive the
4 memory access command and retransmit the memory access command to a next-in-line
5 memory device in the chain.
- 1 43. The method of claim 26 wherein receiving a memory access request that specifies a range

2 of memory address comprises receiving a memory access request that specifies a starting
3 address and a number of storage locations to be accessed.

1 44. A memory device comprising:
2 a first interconnect structure optionally to be coupled to a reference voltage node;
3 a device identifier register; and
4 a control circuit coupled to the first interconnect structure and to the device identifier
5 register, the control circuit being configured to record a first predetermined device
6 identifier in the device identifier register if the first interconnect structure is coupled
7 to the reference voltage node.

1 45. The memory device of claim 44 further comprising a second interconnect structure coupled
2 to the control circuit, and wherein the control circuit is further configured to record a
3 device identifier received via the second interconnect structure if the first interconnect
4 structure is not coupled to the reference voltage node.

1 46. The memory device of claim 45 wherein the first and second interconnect structures each
2 comprise at least one externally accessible contact of the memory device.

1 47. The memory device of claim 44 further comprising a second interconnect structure coupled
2 to the control circuit, and wherein the control circuit is further configured to output a
3 second predetermined device identifier via the second interconnect structure.

1 48. The memory device of claim 47 wherein the second predetermined device identifier is the
2 first predetermined device identifier plus a predetermined increment.

1 49. The memory device of claim 44 further comprising a second interconnect structure coupled
2 to the control circuit, and wherein the control circuit is further configured to output the first
3 predetermined device identifier via the second interconnect structure.

1 50. A method of operation within a memory device, the method comprising:
2 storing a first predetermined device identifier in a storage circuit of the memory device if a
3 configuration signal is in a first state; and
4 storing, in the storage circuit, a device identifier indicated by signals received at an input
5 interface of the memory device if the configuration signal is in a second state.

1 51. The method of claim 50 wherein storing a device identifier indicated by signals received at
2 the input interface of the memory device comprises generating the device identifier by
3 incrementing a value represented by the signals received at the input interface.

1 52. The method of claim 50 further comprising outputting a second predetermined device
2 identifier at an output interface of the memory device if the configuration signal is in the
3 first state.

1 53. The method of claim 52 wherein the second predetermined device identifier is the first
2 predetermined device identifier plus a predetermined increment.

1 54. The method of claim 50 further comprising outputting the first predetermined identifier
2 from the memory device if the configuration signal is in the first state, and outputting the
3 device identifier indicated by the signals received at the input interface if the configuration
4 signal is in the second state.

1 55. The method of claim 50 further comprising outputting from the memory device a device
2 identifier that is the first predetermined identifier plus an increment value if the
3 configuration signal is in the first state, and outputting from the memory device a device
4 identifier that is the device identifier indicated by the signals received at the input interface
5 plus the increment value if the configuration signal is in the second state.

1 56. The method of claim 55 wherein the configuration signal is a single-bit signal.

1 57. A semiconductor memory device comprising:
2 a storage array;
3 an input/output (I/O) interface; and
4 a control circuit coupled to the storage array and to the I/O interface, the storage circuit
5 being configured to retrieve data from the storage array in response to a read
6 command received via the I/O interface and to output the data via the I/O interface in
7 response to an output-enable command received via the I/O interface.

1 58. The memory device of claim 57 further comprising a device identification register to store
2 a device identifier, and wherein the control circuit is further configured to inspect selection
3 information included with the read command to determine whether the device identifier is
4 indicated by device selection information associated with the read command.

1 59. The memory device of claim 58 wherein the device identifier is indicated by the device
2 selection information if the device identifier falls within a range of device identifiers
3 indicated by the device selection information.

1 60. The memory device of claim 58 wherein the device selection information comprises a
2 select value that corresponds to the semiconductor memory device, and wherein the device
3 identifier is indicated by the device selection information if the select value is in a first
4 state.

1 61. The memory device of claim 60 wherein the select value is one of a plurality of bits within
2 the device selection information.

1 62. The memory device of claim 57 wherein the I/O interface comprises an input interface at a
2 first edge of the memory device and an output interface at a second edge of the memory
3 device.

1 63. The memory device of claim 62 wherein the first and second edges of the semiconductor
2 memory device are substantially parallel to one another and disposed on opposite ends of
3 the semiconductor memory device.

1 64. The memory device of claim 57 further comprising a data buffer coupled to the control
2 circuit and the I/O interface, the data buffer being configured to store the data retrieved
3 from the storage array at least until the output-enable command is received.

1 65. The memory device of claim 64 wherein the data buffer comprises a shift register to store a
2 plurality of values that constitute the data retrieved from the storage array.

1 66. The memory device of claim 65 wherein the control circuit is further configured to enable
2 the plurality of values to be shifted, one after another, out of the shift register and the

3 semiconductor memory device in response to receipt of the output-enable command.

1 67. A method of operation within a semiconductor memory device, the method comprising:

2 retrieving data from a storage array in response to a read command;

3 storing the data in a data buffer; and

4 outputting the data from data buffer and the semiconductor memory device in response to

5 an output-enable command.

1 68. The method of claim 67 further comprising receiving the read command at an input

2 interface of the semiconductor memory device and receiving the output-enable command at

3 the input interface a predetermined time after receiving the read command.

1 69. The method of claim 68 wherein the predetermined time corresponds to a data retrieval

2 delay of the semiconductor memory device.

1 70. The method of claim 67 wherein retrieving the data from the storage array in response to

2 the read command comprises retrieving the data from the storage array if a device identifier

3 stored in a configuration circuit of the semiconductor memory device is indicated by device

4 selection information associated with the read command.

1 71. The method of claim 70 wherein retrieving the data from the storage array if the device

2 identifier is indicated by device selection information comprises determining whether the

3 device identifier falls within a range of device identifiers indicated by the device selection

4 information.

1 72. The method of claim 71 wherein the device selection information comprises a select value

2 that corresponds to the semiconductor memory device, and wherein retrieving the data
3 from the storage array if the device identifier is indicated by device selection information
4 comprises determining whether the select value is in a first state.

1 73. The method of claim 72 wherein the select value is one of a plurality of bits within the
2 device selection information.

1 74. The method of claim 67 wherein the data retrieved from the storage array includes a
2 plurality of values, and wherein storing the data in the data buffer comprises storing the
3 plurality of values in a shift register.

1 75. The method of claim 74 wherein outputting the data from the data buffer and the
2 semiconductor memory device in response to the output-enable command comprises
3 shifting the plurality of values, one after another, out of the shift register and the
4 semiconductor memory device in response to receipt of the output-enable command.

1 76. A memory controller comprising:
2 a host interface to receive a memory read request;
3 a memory interface; and
4 a control circuit coupled to the host interface and the memory interface, the control circuit
5 being configured to output a read command via the memory interface in response to
6 the memory read request, delay for a first time interval, then output an data-pickup
7 command via the memory interface to enable receipt of data requested in the memory
8 read request.

1 77. The memory controller of claim 76 wherein the memory read request specifies a range of

2 memory addresses, and wherein the first time interval is determined according to the range
3 of memory addresses.